U.S. DEPARTMENT OF COMMERCE, PATENT AND TRADEMARK OFFICE	DATE: **November 16, 2000**
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371	U.S. AP**09/700575**

INTERNATIONAL APPLICATION NO.: PCT/JP00/01725	INTERNATIONAL FILING DATE: **MARCH 21, 2000**	PRIORITY DATE CLAIMED: **MARCH 23, 1999**

TITLE OF INVENTION: **VIDEO DECODER**

APPLICANT(S) FOR DO/EO/US: **Shigeyuki OKADA**

Applicant hereby submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. **XX** This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ___ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. **XX** This express request to begin national examination procedures (35 USC 371(f)) at any time rather than delay examination until the expiration of the time limit set in 35 USC 371(b) and PCT Articles 22 and 39(1).

4. ___ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. **XX** A copy of the International Application as filed (35 U.S.C. 371(c)(2)):

    a. ___ is transmitted herewith (required only if not transmitted by the International Bureau).
    b. **XX** has been transmitted by the International Bureau.
    c. ___ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. **XX** A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. **XX** Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))

    a. ___ are transmitted herewith (required only if not transmitted by the International Bureau).
    b. ___ have been transmitted by the International Bureau.
    c. ___ have not been made; however, the time limit for making such amendments has NOT expired.
    d. **XX** have not been made and will not be made.

8. ___ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. **XX** An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ___ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

ITEMS 11. TO 16. BELOW CONCERN OTHER DOCUMENT(S) OR INFORMATION INCLUDED:

11. **XX** An Information Disclosure Statement under 37 CFR 1.97 and 1.98 together with the international search report and 5 references.

12. **XX** An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ___ A **FIRST** preliminary amendment.
    ___ A **SECOND** or **SUBSEQUENT** preliminary amendment

14. ___ A substitute specification.

15. ___ A change of power of attorney and/or address letter.

16. **XX** Other items or information: 5 sheets of drawings.

U.S. APPLICATION NO. (if known) 09/700575	INTERNATIONAL APPLICATION NO. PCT/JP00/01725	DATE: November 16, 2000

	CALCULATIONS	PTO USE ONLY
17. X The following fees are submitted:		
Basic National Fee (37 CFR 1.492(a)(1)-(5): Search Report has been prepared by the EPO or JPO: $860.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1000.00		
International preliminary examination fee (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	

Surcharge of **$130.00** for furnishing the oath or declaration later than __ 20 __ 30 months from the earliest claimed priority date (37 DVR 1.492(e)).		

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
TOTAL	11 -20 =		X $ 18.00		
INDEPENDENT	1 - 3 =		X $ 80.00		
Multiple dependent claims(s) (if applicable)		+ $270.00			
			TOTAL OF ABOVE CALCULATIONS =	$ 860.00	
Reduction by 1/2 for filing by small entity, if applicable. (Note 37 CFR 1.9, 1.27, 1.28).					
			SUBTOTAL =	$ 860.00	
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			TOTAL NATIONAL FEE =	$ 860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 per property +**				$ 40.00	
			TOTAL FEES ENCLOSED =	$ 900.00	
				Amount to be: refunded	$
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a. __XX__ A check in the amount of $ __900.00__ to cover the above fees is enclosed. ($860.00 for filing fee and $40.00 for Assignment Recordation fee). (This paper is filed in triplicate)

b. _____ Please charge my Deposit Account No. 01-2340 in the amount of $___ to cover the above fees. (A duplicate copy of this sheet is enclosed.)

c. __X__ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2340.

NOTE: **Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed to request that the application be restored to pending status.**

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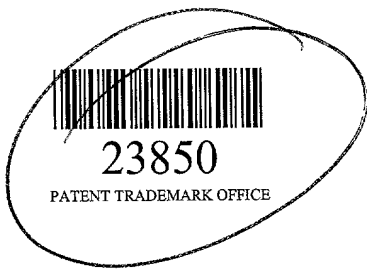
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__Mel R. Quintos__
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__31,898__
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MRQ/yap

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SPECIFICATION

<u>Video Decoder</u>

5   Technical Field

The present invention relates to a video decoder with an image compression system in accordance with, for example, the MPEG standard.

Background Art

10   Multimedia applications handle enormous and various information, and it has been necessary to rapidly process such information for the practical multimedia applications.   A data compression/decompression technology is indispensable for rapidly processing the information.

One example of such a data compression/decompression technology is
15   an "MPEG (Moving Picture Expert Group)" system.   The MPEG system is standardized by an MPEG committee (ISO/IEC JTC1/SC29/WG11) affiliated with ISO (International Organization for Standardization) / IEC (International Electro-technical Commission).

The MPEG consists of three sections.   Part 1, "MPEG systems part,"
20   (ISO/IEC IS 11172 Part 1:Systems) defines multiplex structures and synchronous systems of video data and audio data.   Part 2, "MPEG video part" (ISO/IEC IS 11172 Part 2:Video) defines a high efficiency coding system and a format of video data.   Part 3, "MPEG audio part" (ISO/IEC IS 11172 Part 3:Audio) defines high efficiency coding system and a format
25   of audio data.

The video data handled in the MPEG video part involves a moving image, which is constituted by dozens of (e.g., 30) frames (static images, segments) per second.   The video data is constituted of a six-layer hierarchical structure, which includes a Sequence, a GOP (Group Of
30   Pictures), a Picture, a Slice, a Macroblock and a Block.   The number of Slices forming one Picture may vary, and the number of Macroblocks forming a Slice may also vary.

Further, the MPEG standard defines two systems, MPEG-1 and

MPEG-2, mainly depending on a difference in encoding rates.   In MPEG-1, a frame corresponds to a Picture.   In MPEG-2, a frame or a field may correspond to a Picture.   One frame includes two fields.

It is noted that a structure in which the frame corresponds to a Picture is referred to as a frame structure, whereas a structure in which the field corresponds to a Picture is referred to as a field structure.

The MPEG uses a compression technology called an interframe prediction.   In the interframe prediction, data is compressed based on a time correlation between frames.   A bidirectional prediction is performed in the interframe prediction.   The bidirectional prediction is a prediction that uses a forward prediction predicting a present reconstructed image from a past reconstructed image (or Picture), together with a backward prediction predicting a present reconstructed image from a future reconstructed image.

The bidirectional prediction defines three types of Pictures referred to as an I-Picture (Intra-Picture), P-Picture (Predictive-Picture) and B-Picture (Bidirectionally predictive Picture).

The I-Picture is generated independent of the past or future reconstructed image.   For performing a random access, at least one I-Picture is required in the GOP.   All Macroblock Type within I-Picture are IntraFrame prediction images.

P-Picture is generated by the forward prediction (the prediction from a past I-Picture or P-Picture).   A Macroblock Type within P-Picture includes both IntraFrame prediction image and Forward Inter Frame prediction image.

B-Picture is generated by the bidirectional prediction.   In the bidirectional prediction, B-Picture is generated by any one of the three predictions below.

· Forward prediction; a prediction from a past I-Picture or B-Picture

· Backward prediction; a prediction from a future I-Picture or P-Picture

· Bidirectional prediction; a prediction from past and future I-Picture or P-Picture

The Macroblock within B-Picture includes four types, that is, Intraframe prediction image, Forward Inter Frame prediction image, Backward Inter Frame prediction image, and Interpolative Inter Frame prediction image.

5   These I, P and B Pictures are respectively encoded.   That is, an I-Picture is generated without a past or future Picture.   On the other hand, a P-Picture is generated only when there is a past Picture, and a B-Picture is generated only when there is a future Picture.

However, when the Mactoblock Type is Interpolative Inter Frame,
10   Mactoblocks of P-Picture and B-Picture could be generated even if there is no past or future Picture.

In Inter Frame prediction, initially, an I-Picture is periodically generated.   Subsequently, a frame that is some frames ahead of the I-Picture is generated as a P-Picture.   This P-Picture is generated by a
15   prediction in one-way (in the forward direction) from past to present. Thereafter, a frame located before the I-Picture and after the P-Picture is generated as a B-Picture.   When the B-Picture is generated, a best prediction method is selected from the three predictions, the forward prediction, the backward prediction and the bidirectional prediction.
20   Generally, in a continuous moving image, a present image is similar to preceding/succeeding images, except for only a part.   It is assumed that a frame (e.g., I-Picture) and the succeeding frame (e.g., P-Picture) are almost the same, and if there is a difference between these frames, only the difference (data of B-Picture) is extracted for compression.   This allows the
25   compression to be performed in accordance with time correlation of data between the frames.

A data stream (bit stream) of video data encoded based on the MPEG video part, as described above, is referred to as an MPEG video stream (hereinafter referred to as a video stream).

30   It is noted that MPEG-1 mainly corresponds to storage media such as a video CD (Compact Disc) and a CD-ROM (CD-Read Only Memory). MPEG-2 corresponds, not only to the storage media such as a video CD, a CD-ROM, a DVD (Digital Video Disc), a video tape and a memory card

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using a nonvolatile semiconductor memory, but also to all transmission media including communication media such as LAN (Local Area Network) and broadcasting media such as terrestrial broadcasting, satellite broadcasting and CATV (Community Antenna Television).

5   Motion Compensated prediction (MC) and Discrete Cosine Transform (DCT) are core technologies used in the MPEG video part. A coding technology using both MC and DCT are referred to as a hybrid coding technology. A DCT code is used in the MPEG video part at the time of encoding, to decompose an image (a video signal) into frequency

10   components for processing. Inverse DCT (IDCT) is used at the time of decoding to restore the frequency components to an image.

Fig. 4 is a block circuit diagram of a conventional MPEG video decoder 101.

MPEG video decoder 101 includes a control core circuit 102, a bit

15   buffer 103, a frame buffer 104, an MPEG decode core circuit 105, a data bus 106, a display circuit 107, a memory controller 108 and buffers 109-115 with FIFO (First-In-First-Out) configurations. Circuits 102-115 constituting MPEG video decoder 101 are mounted on one LSI chip.

Control core circuit 102 controls circuits 103-115.

20   A video stream transferred from a transmission medium 130 is initially input to buffer 109, transferred therefrom in the order of data bus 106, memory controller 108 and to bit buffer 103, and written into bit buffer 103. Transmission medium 130 includes a storage medium (i.e., a video CD, a CD-ROM, a DVD, a video tape, a memory card or the like), a

25   communication medium (LAN or the like), and a broadcasting medium (terrestrial broadcasting, satellite broadcasting, CATV or the like).

Bit buffer 103 is constituted of a ring buffer including a SDRAM (Synchronous Dynamic Random Access Memory) with FIFO configuration, and successively stores video streams transmitted from transmission

30   medium 130.

Bit buffer 103 is provided because each of the I-Picture, the P-Picture and the B-Picture has a different data size. The data size of the I-Picture is approximately 30 kilo byte, the data size of the P-Picture is

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approximately 10-15 kilo byte, and the data size of the B-Picture is approximately 0-6 kilo byte.   However, bit rate of the video stream transmitted from transmission medium 130 is constant.   MPEG decode core circuit 105 performs a process for each Picture, and the process time is
5   different depending on the data size of each Picture.   This causes a problem that some Pictures may not be processed in MPEG decode core 105 if the video stream transmitted from transmission medium 130 is directly transferred to MPEG decode core circuit 105.   To prevent such a problem, bit buffer 103 is provided as a buffer memory for the video stream
10   transferred from transmission medium 130, absorbing a difference between data sizes of I-, P- and B-Pictures.

Frame buffer 104 includes an SDRAM, and its inside is divided into three regions (i.e., a forward reference area 120, a rearward reference area 121 and a B-Picture storage area 122).
15   It is noted that bit buffer 103 and frame buffer 104 are provided in different regions in one SDRAM, in order to reduce the number and cost of components in MPEG video decoder 101.

Input/output data bus width (bit width) of the SDAM, in which bit buffer 103 and frame buffer 104 are provided, is set to 32 bit.   Thus,
20   input/output data bus width of memory controller 108 and data bus width of data bus 106 are also set to 32 bit.

Memory controller 108 controls reading and writing operations of bit buffer 103 and frame buffer 104.

The video stream stored in bit buffer 103 is read, by memory
25   controller 108, for each Picture per one frame period, and the read video stream is transferred from memory controller 108 through data bus 106 and buffer 110 in this order, and input into MPEG decode core circuit 105.

For the video stream of one Picture that has been input, MPEG decode core circuit 105 first performs a variable length decoding process
30   based on the Huffman code.   Next, a dequantization process based on a quantization threshold is performed for the result of the variable length decoding process, to obtain a DCT (Discrete Cosine Transform) coefficient. Thereafter, the obtained DCT coefficient is subjected to an IDCT process,

and finally an MC (Motion Compensated prediction) process is performed for the result of IDCT (Inverse DCT) process.

The result of the MC process by MPEG decode core circuit 105 is transferred through buffer 114, data bus 106, memory controller 108 and to frame buffer 104 in this order, and stored in any of the areas 120-122 of frame buffer 104 by memory controller 108.

Further, the data read from each of the areas 120-122 of frame buffer 104 by memory controller 108 is transferred in the order from memory controller 108, data bus 106 and to any one of the buffers 111-113, and is input into MPEG decode core circuit 105. Here, the data read from forward reference area 120 is transferred via buffer 111, the data read from rearward reference area 121 is transferred via buffer 112, and the data read from B-Picture storage area 122 is transferred via buffer 113.

A future I-Picture or P-Picture, used when a backward prediction is performed in the MC process by MPEG decode core circuit 105, is stored in forward reference area 120. A past I-Picture or P-Picture, used when a forward prediction is performed in the MC process, is stored in rearward reference area 121. A B-Picture is stored in B-Picture storage area 122.

I-Picture or P-Picture stored in forward reference area 120 and rearward reference area 121 are used as base data for performing the forward or backward prediction, so that they must be kept stored in the areas 120 and 121. B-Picture stored in B-Picture storage area 122 is not handled as base data, and hence the B-Picture will be unnecessary once it is output to the outside of MPEG video decoder 101. It is noted that areas 120-122 are also referred to as planes.

The Picture data read by memory controller 108 from any one of areas 120-122 of frame buffer 104 is transferred from memory controller 108 through data bus 106 and buffer 115 in this order, and is input into display circuit 107.

Display circuit 107 generates a video signal (an image signal) from the data of the Picture, and outputs the video signal to an external device 131 connected to MPEG video decoder 101. For example, if a display is connected as external device 131, the display displays the video signal as

an image.   If a storage medium (a video tape, a memory card and so forth) is connected as external device 131, the video signal is stored in the storage medium.

MPEG video decoder 101 configured as described above is incorporated into a movie camera, a still camera, a television, a video CD reproducing device, a DVD reproducing device and so forth.   When MPEG video decoder 101 is incorporated into a movie camera or a still camera, transmission medium 130 is replaced by an image pick-up device, such as a CCD (Charge Coupled Device), and the signal processing circuit therefor.

Fig. 5 schematically shows a storing state of luminance (Y) data and color difference (C) data stored in forward reference area 120 and rearward reference area 121 of frame buffer 104 including an SDRAM.

Forward reference region 120A is provided with storage area 140 for forward-reference luminance data yf and a storage area 141 for forward-reference color-difference data cf.   Further, rearward reference area 121 is provided with a storage area 142 for rearward-reference luminance data yr and a storage area 143 for rearward-reference color-difference data cr.

The data size of the color-difference data is approximately half the data size of the luminance data.   The data size of each storage area 141, 143 are set to approximately half the data size of each storage area 140, 142.

It is noted that provision of storage areas 140-143 in areas 120 and 121 of frame buffer 104, for respectively storing data yf, cf, yr and cr therein as described above, is referred to as "memory mapping."

Generally, upon accessing the SDRAM, it is required to set a predetermined command that is determined by a cast sequence and a burst range defined by the SDRAM.   Such setting of the predetermined command is referred to as "command overhead."   Thus, in a period from a time point at which an access starts to a time point at which actual data writing or reading starts, delay time for a time period required for the command overhead occurs.   It is impossible to make this time period required for the command overhead (delay time) equal to or shorter than 6 to 7 operation clocks of the SDRAM.

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Fig. 6 schematically shows the order of the memory access in a case where data for one Macroblock is read from areas 120 and 121 of frame buffer 104 including an SDRAM with an input/output data bus width of 32 bit.

5   The memory access is performed in the order as follows: command overhead com for storage area 140; reading of forward-reference luminance data yf from storage area 140; command overhead com for storage area 141; reading of forward-reference color-difference data cf from storage area 141; command overhead com for storage area 142; reading of rearward-reference

10   luminance data yr from storage area 142; command overhead com for storage area 143; and reading of rearward-reference color-difference data cr from storage area 143.

Therefore, time period T1 required for the memory access in such a case can be obtained by the equation (1) below.

15     $T1 = 4 \times t1 + 2 \times t2 + 2 \times t3$ ...(1), wherein

t1 is a time period required for command overhead com,

t2 is a time period required for reading of luminance data yf, yr, and

t3 is a time period required for reading of color difference data cf, cr.

In the MC process by MPEG decode core circuit 105, for restoring

20   luminance data for half the one Macroblock (half-Macroblock), the luminance data for half-Macroblock may be read from forward reference area 120 or rearward reference area 121.

As shown in Fig. 7, the luminance data that must be read from forward reference area 120 or rearward reference area 121 to restore the

25   luminance data for the half-Macroblock is data of 9 pixels (picture element) × 17 pixels (picture element).

Generally, a minimum unit that can access the SDRAM will be equal to the value of the burst range defined by the SDRAM multiplied by the input/output data bus width.

30   Because the minimum value of the burst range is "2," the minimum unit for accessing the SDRAM having the input/output data bus width of 32 bit will be 2 × 32 bit.   It is noted that data size of one pixel (picture element) is 8 bit.   Therefore, the minimum unit for accessing the SDRAM

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with the input/output data bus width of 32 bit will be horizontally arranged 8 pixels.

Thus, as shown in Fig. 7B, it is necessary to read 9 pixels × 24 pixels of data in order to read the luminance data of the half-Macroblock (9 pixels × 17 pixels of data) from frame buffer 104 including the SDRAM with the input/output data bus width of 32 bit. Thus, data of 24 pixels, i.e., three times the horizontal 8 pixels, must be read in order to read data of horizontal 17 pixels, since the minimum unit for accessing the SDRAM with the input/output data bus width of 32 bit is horizontal 8 pixels. Except for the necessary data of 9 pixels × 17 pixels of the read data of 9 pixels × 24 pixels, the remaining data of 9 pixels × 7 pixels will be unnecessary.

In recent years, faster operation speed of MPEG video decoder 101 is required. For increasing the operation speed, there are a method of speeding up frame buffer 104 and data bus 106 to increase the operation frequency, and a method of further expanding the input/output data bus width (bit width) to be wider than 32 bit (e.g., 48 bit, 64 bit, 128 bit and so forth). However, frame buffer 104 with high operation frequency will have an increased power consumption, in addition to being expensive. (For example, Rambus DRAM faster than the SDRAM will be more expensive than the SDRAM.) Further expansion of input/output data bus width increases the number of terminals in an LSI as well as the number of chips in the SDRAM included in frame buffer 104, causing increase of a substrate mounting area of MPEG video decoder 101 and higher cost. Thus, it has been required to increase the operation speed of MPEG video decoder 101 without making the operation frequency of frame buffer 104 higher or expanding the input/output data bus width.

Disclosure of Invention

It is an object of the present invention to provide a video decoder using an image compression system, such as the MPEG standard, which enables increase of an operation speed.

To achieve such an object, according to an aspect of the present

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invention, a video decoder, decoding a video stream using a discrete cosine transform together with a motion compensated prediction performing a backward prediction and a forward prediction, includes a first frame buffer provided with a storage area for forward-reference luminance data used in the backward prediction and a storage area for rearward-reference color-difference data used in the forward prediction; a second frame buffer provided with a storage area for forward-reference color-difference data used in the forward prediction and a storage area for rearward-reference luminance data used in the forward prediction; and a read control circuit performing at least a part of a memory access operation for the first frame buffer and a memory access operation for the second frame buffer in a parallel processing.

Thus, in the present invention, if the first and second frame buffers with a small input/output data bus width are used, reading of unnecessary data can be reduced even when luminance data of a half-Macroblock (for example, data of 9 pixels × 17 pixels) is read from each frame buffer, which can correspondingly shorten a time period required for memory access. Therefore, the operation speed of the video decoder can be increased without making the operation frequency of each frame buffer higher or expanding the input/output data bus width.

According to another aspect of the present invention, a video decoder, decoding a video stream using a discrete cosine transform together with a motion compensated prediction performing a backward prediction and a forward prediction, includes a first frame buffer provided with a storage area for forward-reference luminance data used in the backward prediction and a storage area for rearward-reference color-difference data used in the forward prediction; a second frame buffer provided with a storage area for forward-reference color-difference data used in the forward prediction and a storage area for rearward-reference luminance data used in the forward prediction; and a read control circuit performing memory accesses for the first frame buffer and the second frame buffer in a parallel processing, to read the forward-reference luminance data from the first frame buffer while reading the forward-reference color-difference data from the second

frame buffer, and also to read the rearward-reference color-difference from the first frame buffer while reading the rearward-reference luminance data from the second frame buffer.

Therefore, according to the present invention, extremely effective shortening of the time period required for the memory access can be attained.

More preferably, the video decoder includes a write control circuit for storing the forward-reference luminance data and the rearward-reference color-difference data into a predetermined storage area in the first frame buffer, and also for storing the forward-reference color-difference data and the rearward-reference luminance data into a predetermined storage area in the second frame buffer.

More preferably, in the video decoder, each of the first and second frame buffers includes an SDRAM with the same input/output data bus width.

Therefore, according to the present invention, memory accesses for the first frame buffer and the second frame buffer are performed in a parallel processing.   Thus, the time period required for the memory access upon reading of the luminance data and the color difference data of one Macroblock from each frame buffer can be shortened for a time period required for two command overheads defined by a buffer memory such as the SDRAM.   Thus, the operation speed of the video decoder can further be increased.

Brief Description of Drawings

Fig. 1 is a block circuit diagram of an MPEG video decoder according to the first embodiment of the present invention;

Fig. 2 is a first schematic diagram illustrating an operation of the first embodiment;

Fig. 3 is a second schematic diagram illustrating an operation of the first embodiment;

Fig. 4 is a block circuit diagram of a conventional MPEG video decoder;

Fig. 5 is a first schematic diagram illustrating an operation of a conventional MPEG video decoder;

Fig. 6 is a second schematic diagram illustrating an operation of a conventional MPEG video decoder; and

Figs. 7A-7C are schematic diagrams illustrating an operation of a conventional MPEG video decoder. Fig. 7A shows data required for restoring luminance data of a half-Macroblock, Fig. 7B shows data read upon reading luminance data of the half-Macroblock from frame buffer 104, and Fig. 7C shows an operation of reading luminance data of the half-Macroblock from the frame buffer.

Best Mode for Carrying Out the Invention

Embodiments of the present invention will be described below with reference to the drawings.

It should be noted that, in the embodiments, same components as the ones in the conventional MPEG video decoder shown in Figs 4-7C are denoted by the same reference characters, and the description thereof will not be repeated.

Fig. 1 is a block circuit diagram showing a configuration of an MPEG video decoder 1 of the first embodiment.

MPEG video decoder 1 includes a control core circuit 2, a switch circuit 3, bit buffers 103a and 103b, frame buffers 104a and 104b, an MPEG decode core circuit 105, data buses 106a and 106b, a display circuit 107, memory controllers 108a and 108b, and buffers with FIFO configurations 109, 110a-115b. Circuits 2 and 103a-115b constituting MPEG decoder 1 are mounted on one LSI chip.

Control core circuit 2 controls circuits 3 and 103a-115b.

A video stream transferred from a transmission medium 130 is initially input into buffer 109, and transferred therefrom through each of data buses 106a, 106b and each of memory controllers 108a, 108b, and to each of bit buffers 103a, 103b, and is written in each of bit buffers 103a, 103b.

Each of bit buffers 103a, 103b is constituted of a ring buffer

including an SDRAM with the FIFO configuration, and successively stores video streams transferred from transmission medium 130.

Bit buffers 130a, 130b are provided for the same reason as why bit buffer 103 is provided in conventional MPEG video decoder 101.

Each of frame buffers 104a, 104b includes the SDRAM, and its inside is divided into three regions (forward reference areas 120a, 120b; rearward reference areas 121a, 121b; and B-Picture storage areas 122a, 122b).

To reduce the number and cost of components in MPEG video decoder 1, bit buffer 103a and frame buffer 104a are provided in different regions of one SDRAM, and bit buffer 103b and frame buffer 104b are provided in different regions of one SDRAM.

Input/output data bus width (bit width) of SDRAMs in which bit buffers 103a, 103b and frame buffers 104a, 104b are respectively provided is set to 16 bit. Correspondingly, input/output data bus width of each of memory controllers 108a, 108b and data bus width of each of data buses 106a, 106b are also set to 16 bit.

Memory controller 108a controls reading and writing operations of bit buffer 103a and frame buffer 104a. Memory controller 108b also controls reading and writing operations of bit buffer 103b and frame buffer 104b.

The video stream stored in each of bit buffers 103a and 103b is read for one Picture per one frame period by each of memory controllers 108a and 108b. The video stream for one Picture read from bit buffer 103a is transferred from memory controller 108a through data bus 106a and buffer 110a in this order, and is input to MPEG decode core circuit 105. Further, the video stream for one Picture read from bit buffer 103b is transferred from memory controller 108b through data bus 106b and buffer 110b in this order, and is input to MPEG decode core circuit 105.

MPEG decode core circuit 105, as in the case with conventional MPEG video decoder 101, successively performs a variable length decoding process, a dequantization process, an IDCT process and an MC process, for the input video stream of one Picture.

The result of the MC process by MPEG decode core circuit 105 is

transferred to switch circuit 3. Switch circuit 3 is switched to either side of each node 3a, 3b. When switch circuit 3 is switched to a node 3a side, the result of the MC process is transferred through buffer 114a, data bus 106a, memory controller 108a and to frame buffer 104a in this order, and is stored in any one of the areas 120a-122a of frame buffer 104a by memory controller 108a. When switch circuit 3 is otherwise switched to a node 3b side, the result of the MC process is transferred from buffer 114b, data bus 106b, memory controller 108b and frame buffer 104b in this order, and is stored in any one of the areas 120b-122b of frame buffer 104b by memory controller 108b.

The data read from each area 120a-122a of frame buffer 104a by memory controller 108a is transferred from memory controller 108a through data bus 106a and any one of buffers 111a-113a in this order, and is input to MPEG decode core circuit 105. Here, the data read from forward reference area 120a is transferred via buffer 111a, the data read from rearward reference area 121a is transferred via buffer 112a, and the data read from B-Picture storage area 122a is transferred via buffer 113a.

Further, the data read from each of the areas 120b-122b of frame buffer 104b is transferred from memory controller 108b through data bus 106b and any of buffers 111b-113b in this order, and is input to MPEG decode core circuit 105. Here, the data read from forward reference area 120b is transferred via buffer 111b, the data read from rearward reference area 121b is transferred via buffer 112b, and the data read from B-Picture storage area 122b is transferred via buffer 113b.

A future I-Picture or P-Picture, used upon the backward prediction in the MC process by MPEG decode core circuit 105, is stored in each of forward reference areas 120a and 120b. A past I-Picture or P-Picture, used upon the forward prediction in the MC process, is stored in each of rearward reference areas 121a and 121b. A B-Picture is stored in each of B-Picture storage areas 122a and 122b.

The I-Picture or P-Picture stored in each of forward reference areas 120a, 120b and in each of rearward reference areas 121a, 121b is used as base data for performing the forward prediction or the backward prediction,

and hence it must be kept stored in each of areas 120a, 120b, 121a and 121b until it is no longer necessary. The B-Picture stored in B-picture storage regions 122a, 122b are not used as base data, so that the B-picture will be unnecessary once it is output to the outside of MPEG video decoder 1. It is noted that each of areas 120a-122b is also referred to as a plane.

Then, the Picture data read from any one of the areas 120a-122a of frame buffer 104a by memory controller 108a is transferred from memory controller 108a through data bus 106a and buffer 115a in this order, and is input to display circuit 107.

Further, the Picture data read from any one of the areas 120b-122b by memory controller 108b is transferred from memory controller 108b through data bus 106b and buffer 115b in this order, and is input to display circuit 107.

Display circuit 107 generates a video signal (an image signal) from the Picture data transferred from each of buffers 115a, 115b, and outputs the video signal to an external device 131 connected to MPEG video decoder 1.

MPEG video decoder 1 configured as described above is incorporated, as in the case with conventional MPEG video decoder 101, into a movie camera, a still camera, a television, a video CD reproducing device and a DVD reproducing device. When MPEG video decoder 1 is incorporated into a movie camera or a still camera, transmission medium 130 is replaced with an image pick-up device, such as a CCD, and its signal processing circuit.

Fig. 2 schematically shows a storage state of luminance (Y) data and color difference (C) data stored in forward reference areas 120a, 120b and rearward reference areas 121a, 121b of respective frame buffers 104a, 104b including SDRAMs.

In frame buffer 104a, a storage area 140 for forward-reference luminance data yf is provided in forward reference area 120a, whereas a storage area 143 for rearward-reference color-difference data cr is provided in rearward reference area 121a.

In frame buffer 104b, a storage area 141 for forward-reference color-

difference data cf is provided in forward reference area 120b, whereas a storage area 142 for rearward-reference luminance data yr is provided in rearward reference area 121b.

As described above, data size of color difference data is approximately half the data size of luminance data, and hence data size of each of storage areas 141, 143 are set to approximately half the data size of each of storage areas 140, 142.

Thus, storing of each data yf, cr, cf and yr into respective areas 120a, 121a, 120b and 121b of frame buffers 104a and 104b can be more easily and securely performed by switching operation of the switch circuit 3.

It is noted that provision of storage regions 140-143 for respectively storing data yf, cf, yr and cr in areas 120a, 121a, 120b and 121b of frame buffers 104a, 104b are referred to as memory mapping.

Fig. 3 schematically shows an order of memory access in a case where data of one Macroblock is read from each of areas 120a, 121a, 120b, 121b of frame buffers 104a, 104b including SDRAMs with the input/output data bus width of 16 bit.

The memory access for frame buffer 104a is performed in the following order: command overhead com for storage area 140; reading of forward-reference luminance data yf from storage area 140; command overhead com for storage area 143; and reading of rearward-reference color-difference data cr from storage area 143.

The memory access for frame buffer 104b is performed in the following order: command overhead com for storage area 141; reading of forward-reference color-difference data cf from storage area 141; command overhead com for storage area 142; and reading of rearward-reference luminance data yf from storage area 142.

Thus, forward-reference luminance data yf read from storage area 140 is transferred, while forward-reference color-difference data cf read from storage area 141 is transferred to MPEG decode core circuit 105. Thus, as in the case with conventional MPEG video decoder 101, MPEG decode core circuit 105 performs the backward prediction by the MC process, based on forward-reference luminance data yf and forward-reference color-

difference data cf.

Further, rearward-reference color-difference data cf read from storage area 143 is transferred, while rearward-reference luminance data yr read from storage area 142 is transferred to MPEG decode core circuit 105. Thus, as in the case with conventional MPEG video decoder 101, MPEG decode core circuit 105 performs the forward prediction by the MC process, based on rearward-reference color-difference data cr and rearward-reference luminance data yr.

Frame buffers 104a and 104b; memory controllers 108a and 108b; and buffers 111a, 112a and buffers 111b, 112b respectively operate at the same time, and thus memory accesses for frame buffers 104a, 104b are performed in the parallel processing.

Therefore, time period T2 required for the memory access in such a case can be obtained by the equation (2) below.

$$T2 = 2 \times t1 + t4 + t5 \qquad ...(2), \text{ wherein}$$

t1 is a time period required for command overhead com,

t4 is a time period required for reading of luminance data yf, yr, and

t5 is a time period required for reading of color difference data cf, cr.

Here, the data bus width of each of frame buffers 104a, 104b is 16 bit. By contrast, the data bus width of frame buffer 104 in conventional MPEG video decoder 101 is 32 bit. Thus, relation between the time t1, t3, t4 and t5 is shown in equation (3) below.

$$t4 = 2 \times t2$$
$$t5 = 2 \times t3 \qquad ...(3)$$

As a result, relation between time T1 required for the memory access for conventional MPEG video decoder 101 obtained by the earlier equation (1) and time T2 required for the memory access for MPEG video decoder 1 of the present invention is shown in equation (4) below.

$$T2 = T1 - 2 \times t1 \qquad ...(4)$$

Therefore, according to MPEG video decoder 1 of the present invention, the time period required for the memory access upon reading the luminance data and the color difference data of one Macroblock from frame buffers 104a, 104b can be made shorter for a time period required for two

command overheads com (= 2 × t1), compared to conventional MPEG video decoder 101.

As shown in Fig. 7C, it is only necessary to read data of 9 pixels × 20 pixels in order to read the luminance data of half-Macroblock (data of 9 pixels × 17 pixels) from each of frame buffers 104a, 104b including SDRAM with the input/output data bus of 16 bit. The minimum unit for accessing the SDRAM with the input/output data bus width of 16 bit is horizontal 4 pixels, and thus it is only necessary to read the data of 20 pixels, i.e., five times the horizontal 4 pixels, in order to read the data of horizontal 17 pixels. Then, if necessary data of 9 pixels × 17 pixels is subtracted from the read data of 9 pixels × 20 pixels, the remaining data of 9 pixels × 3 pixels will be unnecessary.

As described above, in conventional MPEG video decoder 101, 9 pixels × 24 pixels of data must be read, and thus data of 9 pixels × 7 pixels will be unnecessary after subtracting necessary data of 9 pixels × 17 pixels.

Therefore, according to MPEG video decoder 1 of the present invention, compared to conventional MPEG video decoder 101, it will be unnecessary to read an amount of useless 9 pixels × 4 pixels of data upon reading the luminance data of half-Macroblock from frame buffers 104a and 104b, shorting the time required for the memory access for that amount.

As has been described, according to MPEG video decoder 1 of the present invention, the time period required for memory access upon reading data from frame buffers 104a, 104b can be shortened, compared to conventional MPEG video decoder 101, when the MC process is performed in MPEG decode core circuit 105.

Therefore, according to the present invention, the operation speed of MPEG video decoder 1 can be increased without further making the operation frequency of frame buffers 104a, 104b higher or expanding the input/output data bus width. It should be noted that the operation speed of MPEG video decoder 1 of the present invention is 1.3-1.5 times faster than that of conventional MPEG video decoder 101.

Thus, MPEG video decoder 1 with increased operation speed can be

realized, without expensive and power-consuming frame buffers 104a, 104b with high operation frequency, resulting in that the increase of cost and power consumption can be avoided upon increase of the operation speed of MPEG video decoder 1.

5   In the present invention, data bus width (bit width) of SDRAM constituting frame buffers 104a and 104b, memory controllers 108a and 108b, and data buses 106a and 106b are all set to 16 bit, and thus the total of 32 bit, i.e., 16 bit + 16 bit can be attained. When a process with even higher speed is required, 64 bit will be required, which can be attained by

10   setting all the data bus width of SDRAM constituting frame buffers 104a and 104b, memory controllers 108a and 108b, and data buses 106a and 106b to 32 bit, so that the total of 64 bit, i.e., 32 bit + 32 bit can be attained, which will have an effect similar to that of the present invention.

It should be noted that the present invention is not limited to the

15   embodiments described above, and modifications can be made as described below to attain an operation effect equal to or better than the embodiments described above.

(1)   In MPEG video decoder 1, buffers 113a, 113b may be appropriately dispensed with. Further, buffers 111a and 112a may be

20   functionally replaced by one buffer, and buffers 111b and 112b may also be functionally replaced by one buffer.

(2)   Each of frame buffers 104a, 104b can include, instead of SDRAM, a rewritable semiconductor memory in another form (e.g., DRAM, Rambus DRAM or the like).

25   Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

CLAIMS

1.   A video decoder decoding a video stream using a motion
compensated prediction performing a backward prediction and a forward
prediction, comprising:
        a first frame buffer provided with a storage area for forward-
reference luminance data used for said backward prediction and a storage
area for rearward-reference color-difference data used for said forward
prediction;
        a second frame buffer provided with a storage area for forward-
reference color-difference data used for said backward prediction and a
storage area for rearward-reference luminance data used for said forward
prediction; and
        a control circuit for controlling an operation of said video decoder;
        said control circuit performing at least a part of a memory access
operation for said first frame buffer and a memory access operation for said
second frame buffer in a parallel processing.

2.   The video decoder according to claim 1, further comprising:
        a discrete cosine transform processing circuit for processing inverse
discrete cosine transform for decoding data read from said first and second
frame buffers.

3.   The video decoder according to claim 1, wherein said control
circuit stores, in a writing operation, forward-reference luminance data and
rearward-reference color-difference data into a predetermined storage area
in said first frame buffer, and also stores forward-reference color-difference
data and rearward-reference luminance data into a predetermined storage
area in said second frame buffer.

4.   The video decoder according to claim 3, wherein said first and
second frame buffers respectively include first and second memory circuits
in which data output starts a predetermined time period after a read

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command is applied.

5. The video decoder according to claim 4, wherein each of said first and second memory circuits includes a synchronous dynamic random access memory with a same input/output data bus width.

6. The video decoder according to claim 4, wherein said video stream is an MPEG video stream using a discrete cosine transform together with a motion compensated prediction performing backward and forward predictions.

7. The video decoder according to claim 1, wherein said control circuit performs, in a reading operation, memory accesses for said first frame buffer and said second frame buffer in a parallel processing, and controls the reading operation such that
   i) forward-reference luminance data is read from said first frame buffer while forward-reference color-difference data is read from said second frame buffer, and
   ii) rearward-reference color-difference data is read from said first frame buffer while rearward-reference luminance data is read from said second frame buffer.

8. The video decoder according to claim 7, wherein said control circuit stores, in a writing operation, forward-reference luminance data and rearward-reference color-difference data into a predetermined storage area in said first frame buffer, and also stores forward-reference color-difference data and rearward-reference luminance data into a predetermined storage area in said second frame buffer.

9. The video decoder according to claim 8, wherein said first and second frame buffers respectively include first and second memory circuits in which data output starts a predetermined time period after a read command is applied.

10.   The video decoder according to claim 9, wherein each of said first and second memory circuits includes a synchronous dynamic random access memory with a same input/output data bus width.

5

11.   The video decoder according to claim 9, wherein said video stream is an MPEG video stream using a discrete cosine transform together with a motion compensated prediction for backward and forward predictions.

ABSTRACT

An MPEG video decoder 1 decodes a MPEG video stream using a discrete cosine transform together with a motion compensated prediction performing backward prediction and forward prediction. A frame buffer 104a is provided with a storage area for forward-reference luminance data used for the backward prediction and a storage area for rearward-reference color-difference data used for the forward prediction. A frame buffer 104b is provided with a storage area for forward-reference color-difference data used for the backward prediction and a storage area for rearward-reference luminance data used for the forward prediction. Memory access for each of the frame buffers 104a, 104b with an input/output data bus width of 16 bit is performed in a parallel processing.
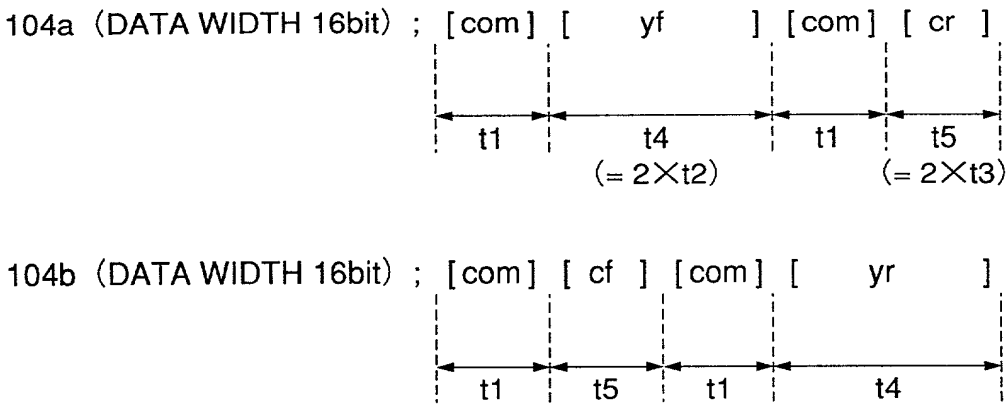
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FIG. 1

FIG. 2

(DATA WIDTH 16bit)

yf —140 } 120a
cr —143 } 121a } 104a
—122a

(DATA WIDTH 16bit)

cf —141 } 120b
yr —142 } 121b } 104b
—122b

FIG. 3

104a (DATA WIDTH 16bit) ; [com] [yf] [com] [cr]

t1 ← t4 → t1 ← t5 →
(=2×t2) (=2×t3)

104b (DATA WIDTH 16bit) ; [com] [cf] [com] [yr]

t1 t5 t1 t4
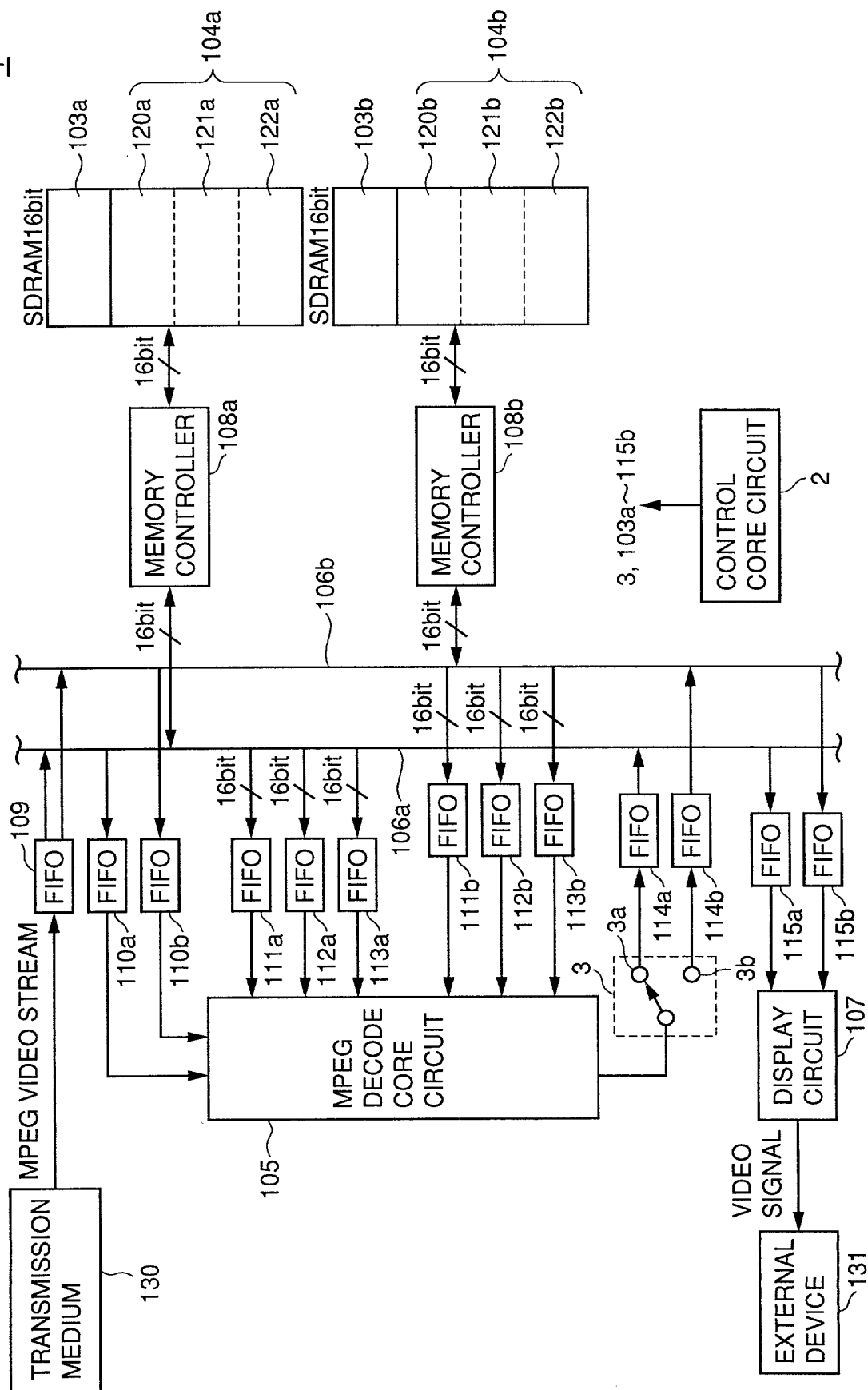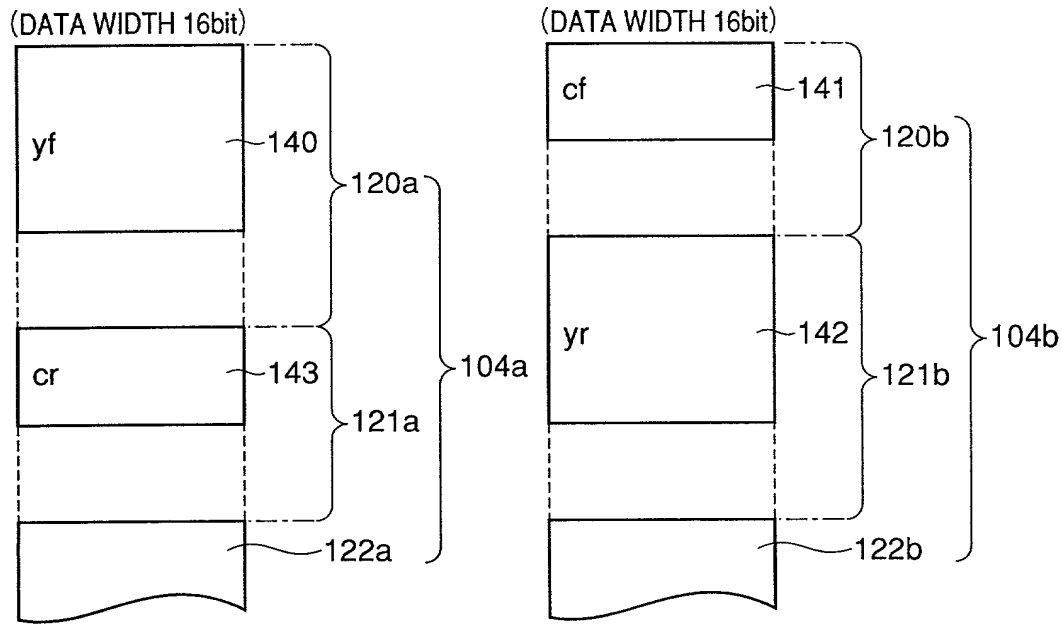
FIG. 4   PRIOR ART

FIG. 5
PRIOR ART   (DATA WIDTH 32bit)
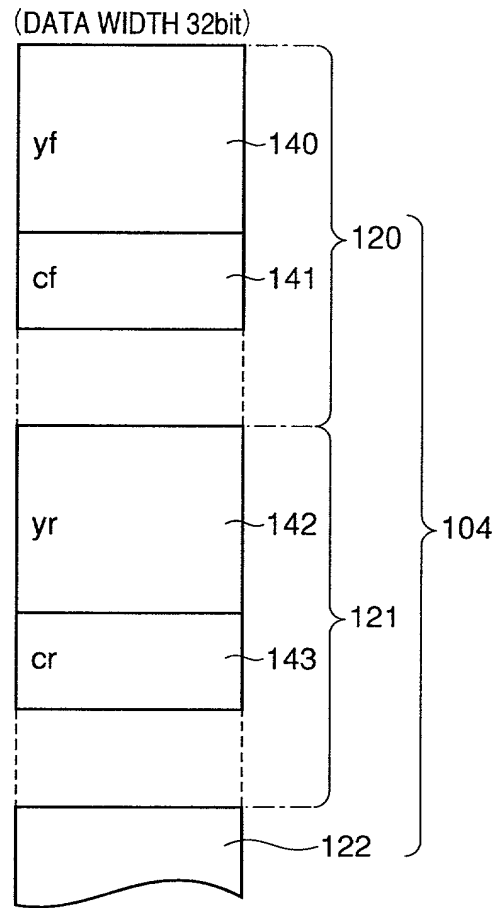
yf   ~140

cf   ~141

}120

yr   ~142

cr   ~143

}121

}104

~122

FIG. 6   PRIOR ART

104 (DATA WIDTH 32bit) ; [com] [yf] [com] [cf] [com] [yr] [com] [cr]

| t1 | t2 | t1 | t3 | t1 | t2 | t1 | t3 |

FIG. 7A
PRIOR ART

17 PIXEL

9 PIXEL

FIG. 7B
PRIOR ART

24

8　　　8　　　8

9

1　　7

UNNECESSARY DATA
(= 9×7)

FIG. 7C
PRIOR ART

20

4　4　4　4　4

9

1　3

UNNECESSARY DATA
(= 9×3)
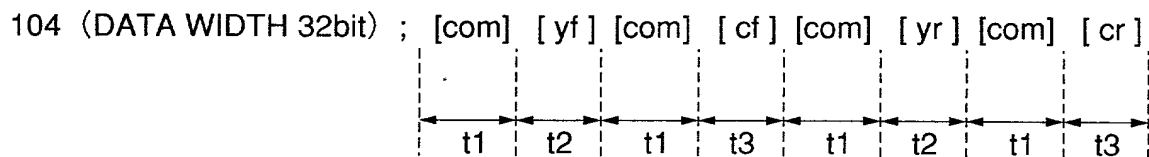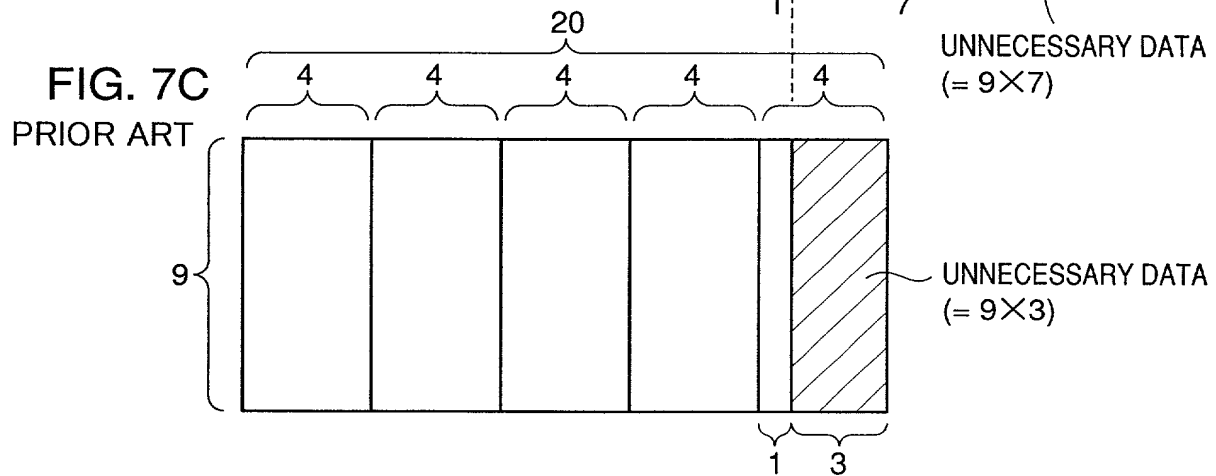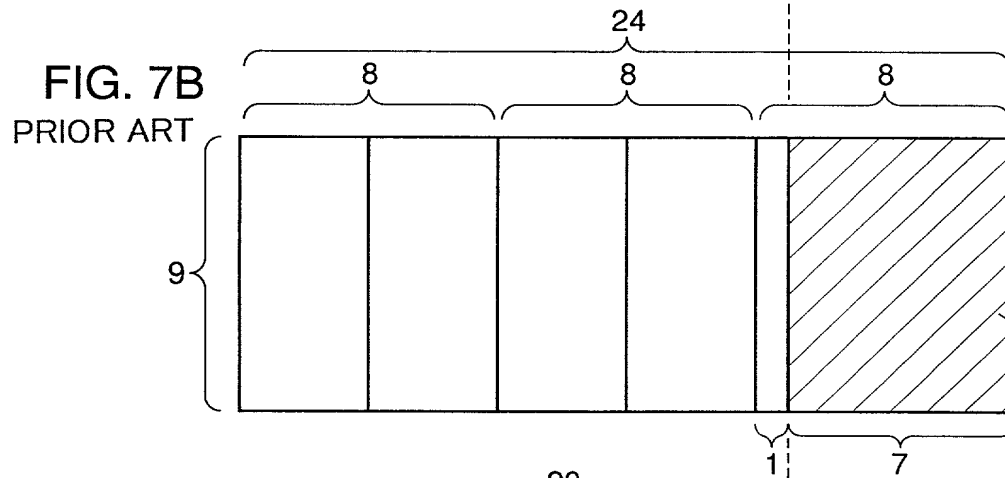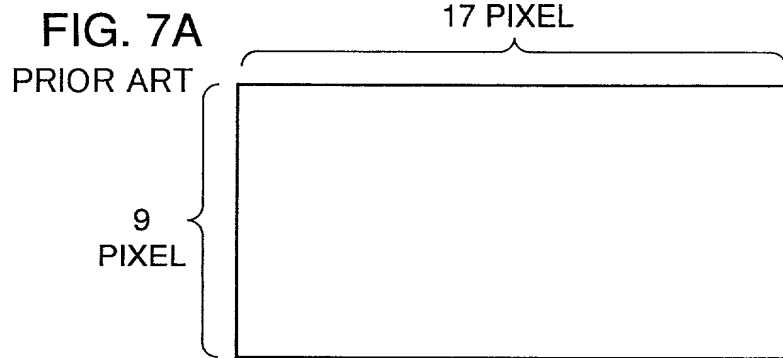
Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **entitled** (Insert Title) ____Video Decoder_____

the specification of which is attached hereto unless the following is checked:

☐ was filed on ___March 21, 2000_____as United States Application Number or PCT International Application Number___PCT/JP00/01725_____and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a) - (d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

				Priority Claimed
(List prior foreign applications. See note A on back of this page)	____11-078207____ (Number)	___Japan___ (Country)	__23/March/1999__ (Day/Month/Year Filed)	☒ Yes ☐ No
	_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No
	_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No
	_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No

(See note B on back of this page)   ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of the application:

(List Prior U.S. Applications)	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)
	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Inventor's Signature___ Date ___

Residence___ Citizenship ___

Post Office Address ___

Full name of third inventor (given name, family name) ___

Inventor's Signature___ Date ___

Residence___ Citizenship ___

Post Office Address ___

Full name of fourth inventor (given name, family name) ___

Inventor's Signature___ Date ___

Residence___ Citizenship ___

Post Office Address ___

Full name of fifth inventor (given name, family name)___

Inventor's Signature___ Date ___

Residence___ Citizenship ___

Post Office Address ___

Full name of sixth inventor (given name, family name) ___

Inventor's Signature___ Date ___

Residence___ Citizenship ___

Post Office Address ___

Full name of seventh inventor (given name, family name) ___

Inventor's Signature___ Date ___

Residence___ Citizenship ___

Post Office Address ___

Full name of eighth inventor (given name, family name) ___

Inventor's Signature___ Date ___

Residence___ Citizenship ___

Post Office Address ___